Notice of Allowability	Application No.	Applicant(s)	
	09/708,435	HUANG, HONG YI	
	Examiner	Art Unit	
	Jean B. Corrielus	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/31/05*.

2. ☒ The allowed claim(s) is/are *1-17,19,20 and 22-26, renumbered as 1-24, respectively*.

3. ☒ The drawings filed on *09 November 2000* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/15/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Jean B Corrielus
Primary Examiner
Art Unit: 2637 8/20/05

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Joe Muncy on 7/11/05.

The application has been amended as follows:

IN THE CLAIMS:

Claims 2-4, 9, 22 and 23 have been amended as follow:

2. (Amended) The signal receiver as claimed in claim 1, wherein the coupling circuit includes a first coupling circuit and a second coupling circuit, the first coupling circuit comprising:

a first transistor [of a first type]; and

a second transistor [of a second type], wherein the gates of the first transistor and the second transistor are coupled to a first terminal of the differential output terminal pair, sources of the first transistor and the second transistor are coupled to a first terminal of the differential input terminal pair, and a drain of the first transistor serves as a first terminal of the external differential input terminal pair; and

[and] the second coupling circuit comprising:

a third transistor [of the first type]; and

a fourth transistor [of the second type], wherein gates of the third transistor and the fourth transistor are coupled together to a second terminal of the differential output terminal pair, sources of the third transistor and fourth transistor are coupled together to a second terminal of the differential input pair, and a drain of the third transistor serves as a second terminal of the external differential input terminal pair.

3. (Amended) The signal receiver as claimed in claim 2, wherein the first and the third [type] transistors are PMOS transistors, the second and fourth [type] transistors are NMOS transistors, and drains of the second transistor and the fourth transistor are connected to [the] ground.

4. (Amended) The signal receiver as claimed in claim 2, wherein the first and third [type] transistors are PMOS transistors, the second and fourth [type] transistors are NMOS transistors, and drains of the second transistor and the fourth transistor are connected to a high voltage.

Claim 9, line 3, "second" has been deleted; line 4, before control, "a" has been replaced by --the--.

22. (Currently Amended) A signal transmitter for transmitting a differential input signal pair to a transmission line, comprising:

an external differential output terminal connecting to the transmission line; and a

control circuit, controlled by a first control signal for defining a first time point for pre-charging the transmission line to a predetermined voltage level via the external differential output terminal before the first time point, and transmitting the differential input signal pair to the transmission line after the first time point, wherein the control circuit includes:

[a first logic gate having an input terminal pair coupled to the first control signal and a first signal of the differential input signal pair, and an output terminal coupled to a first terminal of the external differential output terminal, for pre-charging a first path of the transmission line to the predetermined voltage level via the first terminal of the external differential output terminal before the first time point, and substantially transmitting the first signal of the differential input signal pair to the first path of the transmission line after the first time point; and

a second logic gate having an input terminal pair coupled to the first control signal and a second signal of the differential input signal pair, and an output terminal coupled to a second terminal of the external differential output terminals for pre-charging a second path of the transmission line to the predetermined voltage level via the second terminal of the external differential output terminal before the first time point; and substantially transmitting the second signal of the differential input signal pair to the second path of the transmission line after the first time point;

wherein the control circuit substantially cuts off the interconnection between the differential input signal pair and the transmission line within a predetermined period after the first time point;

wherein the control circuit includes:]

a first differential circuit having an input terminal pair connected to the first control signal and the external differential output terminal, and an output terminal pair for outputting a feedback signal pair; and

a second differential circuit having an input terminal pair connected to the first control signal, the differential input signal pair and feedback signal pair, and an output terminal pair connected to the external differential input terminal;

wherein the control circuit substantially cuts off the interconnection between the differential input signal pair and the transmission line within a predetermined period after the first time point.

23. (Currently Amended) A signal transmitter for transmitting a differential input signal pair to a transmission line, comprising:

an external differential output terminal connecting to the transmission line; and a

control circuit, controlled by a first control signal for defining a first time point for pre-charging the transmission line to a predetermined voltage level via the external differential output terminal before the first time point, and transmitting the differential input signal pair to the transmission line after the first time point, [wherein the control circuit includes:

a first logic gate having an input terminal pair coupled to the first control signal and a first signal of the differential input signal pair, and an output terminal coupled to a first terminal of the external differential output terminal, for pre-charging a first path of the transmission line to the predetermined voltage level via the first terminal of the external differential output terminal before the first time point, and substantially transmitting the first signal of the differential input signal pair to the first path of the transmission line after the first time point; and

a second logic gate having an input terminal pair coupled to the first control signal and a second signal of the differential input signal pair, and an output terminal coupled to a second terminal of the external differential output terminals for pre-charging a second path of the transmission line to the predetermined voltage level via the second terminal of the external differential output terminal before the first time point, and substantially transmitting the second signal of the differential input signal pair to the second path of the transmission line after the first time point;

wherein the control circuit substantially cuts off the interconnection between the differential input signal pair and the transmission line within a predetermined period after the first time point;]

wherein the control circuit comprises:

a first logic gate having an input terminal connected to the first control signal, a first signal of the differential input signal pair and a first feedback signal, and an output terminal connected to a first terminal of the external differential output terminal;

a second logic gate having an input terminal connected to the first control signal, a second signal of the differential input signal pair and a second feedback signal, and an output terminal connected to a second terminal of the external differential output terminal;

a third logic gate having an input terminal connected to the first control signal and the first terminal of the external differential output terminal, and an output terminal for outputting the first feedback signal; and

a fourth logic gate having an input terminal connected to the first control signal and the second terminal of the external differential output terminal, and an output terminal for outputting the second feedback signal;

wherein the control circuit substantially cuts off the interconnection between the differential input signal pair and the transmission line within a predetermined period after the first time point.

Reasons for allowance

The following is an examiner's statement of reasons for allowance: an apparatus signal reception and/or signal reception is disclosed. The closest prior art, Kanazawa et al, US patent no. 5,495,186, discloses similar apparatus. However, Kanazawa et al does not teach or fairly suggest the limitations recited in claim 1,lines 11-16; claim 10, lines 10-15; claim 15, lines 8-20; claim 22, the limitations of" a control circuit including:

a first differential circuit having an input terminal pair connected to the first control signal and the external differential output terminal, and an output terminal pair for outputting a feedback signal pair; and a second differential circuit having an input

terminal pair connected to the first control signal, the differential input signal pair and feedback signal pair, and an output terminal pair connected to the external differential input terminal; wherein the control circuit substantially cuts off the interconnection between the differential input signal pair and the transmission line within a predetermined period after the first time point"; claim 23, the limitations of "a control circuit comprising: a first logic gate having an input terminal connected to the first control signal, a first signal of the differential input signal pair and a first feedback signal, and an output terminal connected to a first terminal of the external differential output terminal; a second logic gate having an input terminal connected to the first control signal, a second signal of the differential input signal pair and a second feedback signal, and an output terminal connected to a second terminal of the external differential output terminal; a third logic gate having an input terminal connected to the first control signal and the first terminal of the external differential output terminal, and an output terminal for outputting the first feedback signal; and a fourth logic gate having an input terminal connected to the first control signal and the second terminal of the external differential output terminal, and an output terminal for outputting the second feedback signal", in combination with the other claimed limitations, are neither anticipated nor rendered obvious by Kanazawa et al.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B Corrielus whose telephone number is 571-272-3020. The examiner can normally be reached on Maxi-Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-3086. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean B Corrielus
Primary Examiner
Art Unit 2637 8/20/05